Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 11 requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock", "a direct modulator operational in response to a modulating data signal and a phase error to generate the OTW" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the modulating data signal to generate the phase error**".

Independent Claim 12 requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock, the digitally-controlled oscillator comprising a voltage controlled oscillator and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW", "a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the modulating data signal to generate the filtered phase error**".

Independent Claim 13 requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock", "a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW, said direct modulator comprising a combinational element feeding the digitally controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior" and "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the modulating data signal to generate the filtered phase error**"

Independent Claim 14 requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to

generate an oscillator clock", "a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW", "a phase-locked loop (PLL) operational in response to **a channel selection signal AND the modulating data signal to generate the filtered phase error**" and "a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL".

In contrast, the circuit disclosed by Fourtet comprises two PLL-based frequency synthesizers: "main synthesizer" (152, 252) and "auxiliary synthesizer" (155, 255). The main synthesizer is used as a "reference signal generator" (154, 254), whereas the auxiliary synthesizer is used as a "frequency modulator" (150, 250). The principle of operation of the frequency modulator is to apply the modulation data signal to the VCO of the main synthesizer and also to the reference signal with the correct balance between the two paths.

Further, Fourtet uses the auxiliary PLL-based synthesizer to create the frequency-modulated reference signal, Fr, by the modulating data 151. This Fr signal is then used as a frequency reference input of the main PLL-based synthesizer. While it is the main PLL in Fourtet which is responsive to the channel selection signal, it is the auxiliary PLL in Fourtet, not the main PLL, which is responsive to the modulating data signal. Further, considering the second feed of the modulating data 151, it should be clarified that it is the VCO 160, not the PLL-based frequency synthesizer 150 that is responsive to the modulating data 151. As a result, Fourtet does not suggest a solution with only one PLL, which has the advantages of being more cost and power efficient. In contrast, the present invention requires "a PLL" to be "operational in response to **a channel selection signal AND the modulating data signal to generate the filtered phase error**" Accordingly, Fourtet fails to teach or suggest the third element of independent Claims 11-14: "**a phase-locked loop** (PLL) operational in response to **a channel selection signal AND the modulating data signal to generate the filtered phase error**". The 35 U.S.C. 103(a) rejection is overcome.

limitation not taught or suggested by the references of record.

Claim 15 further defines the phase-locked loop system according to claim 14 wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator. The Fourtet reference fails to teach or suggest this additional requirement in combination with the previously discussed requirements of Claim 14.

Claim 24 further defines the phase-locked loop system according to claim 11 wherein said phase error is a filtered phase error. The Fourtet reference fails to teach or suggest this additional requirement in combination with the previously discussed requirements of Claim 11.

Claims 1-10, 17-23 and 25 stand allowed. Objected to Claim 16 has been rewritten in independent forming including all of the limitations of the base claim and any intervening claim and therefore stands allowable. Claims 11-15 and 24 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE CLAIMS** – (marked-up copy):

12. (twice amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock, the digitally-controlled oscillator comprising a voltage controlled oscillator[;] and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

16. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW;

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error; and

a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator and [The phase-locked system according to claim 15] wherein the transfer path gain is dependent upon a reference frequency $f_{ref}$ and an estimated digitally-controlled oscillator gain $\hat{K}_{DCO}$, is functionally defined as $\frac{f_{ref}}{\hat{K}_{DCO}}$.